1. (Currently Amended) A silicon-on-insulator integrated structure comprising:

at least one active region comprising active devices;

at least one bulk region adapted to provide structural support to said active region; and

at least one decoupling capacitor, wherein said decoupling capacitor includes capacitive fingers extending into said bulk region, and wherein said decoupling capacitor is outside said active region.

2. (Original) The structure in claim 1, further comprising one or more common lower plates in said bulk region below said capacitive fingers of said decoupling capacitors.

3. (Original) The structure in claim 1, wherein said capacitive fingers comprise one or more trenches lined with an insulator and filled with a conductor.

4. (Original) The structure in claim 3, further comprising an upper plate connected to said conductor within said capacitive fingers.

5. (Original) The structure in claim 4, wherein said upper plate extends from said decoupling capacitor into said active region.

6. (Original) The structure in claim 1, further comprising a bulk contact adapted to bias said bulk region.

7. (Original) The structure in claim 1, wherein said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.

8. (Currently Amended) A silicon-on-insulator integrated structure comprising:

at least one active region comprising active switching devices;

at least one bulk region adapted to provide structural support to said active region, said bulk region being devoid of active switching devices; and

at least one decoupling capacitor, wherein said decoupling capacitor includes capacitive fingers extending vertically into said bulk region in a direction perpendicular to the horizontal upper surface of said bulk region, and wherein said decoupling capacitor is outside said active region.

9. (Original) The structure in claim 8, further comprising a common lower plate in said bulk region below said capacitive fingers of said decoupling capacitors.

10. (Original) The structure in claim 8, wherein said capacitive fingers comprise trenches lined with an insulator and filled with a conductor.

11. (Original) The structure in claim 10, further comprising an upper plate connected to said conductor within said capacitive fingers.

12. (Original) The structure in claim 11, wherein said upper plate extends from said decoupling capacitor into said active region.

13. (Original) The structure in claim 8, further comprising a bulk contact adapted to bias said bulk region.

14. (Original) The structure in claim 8, wherein said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.

15-26. (Canceled).

27. (New) A silicon-on-insulator integrated structure comprising:

at least one active region comprising active devices;

at least one bulk region adapted to provide structural support to said active region;

at least one decoupling capacitor, wherein said decoupling capacitor includes capacitive fingers extending into said bulk region, wherein said capacitive fingers comprise one or more trenches lined with an insulator and filled with a conductor, and wherein said decoupling capacitor is outside said active region; and

an upper plate connected to said conductor within said capacitive fingers, wherein said upper plate extends from said decoupling capacitor into said active region.

28. (New) The structure in claim 27, further comprising one or more common lower plates in said bulk region below said capacitive fingers of said decoupling capacitors.

29. (New) The structure in claim 27, further comprising a bulk contact adapted to bias said bulk region.

30. (New) The structure in claim 27, wherein said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.